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| **Measurement Report : MVBIP ESD EMD Driver Performance on the Custom Prototype** | | | | | | |

# 1 Purpose

Documentation of the driver performance for the custom MVBIP EMD-ESD circuitry on the functional prototype. The results shall be used as an aid to improve the second prototype run and to decide for the optimum RS485 half duplex driver.

## 1.1 Audience

Engineers for hardware development and engineering. Project management. A basic understanding of the MVB [1][2] functionality and signal integrity is required.

# 2 Summary

The function prototype for the MVB [1] physical layer driver features a hardware configuration options [3] that allows the selection for MVB ESD or MVB EMD drive mode [1]. This unique feature requires care in selecting the optimum RS485 driver circuitry and an appropriate layout in terms of high frequency signal integrity. The same RS485 half-duplex device driver shall be used to drive the biased RS485 like bus segment in MVB ESD mode as well as the transformer based circuitry for the MVB EMD mode [1].

A minimal test setup has been identified that allows for different performance measurements of the driver circuitry. Two different RS485 half duplex driver chips from the semiconductor market have been identified that share the same industry standard pinout for RS485 driver chips and do provide enough voltage margin to drive ESD as well as EMD [1][2][5][6].

For the same nominal load the ESD mode requires more drive strength than EMD. The ESD differential lines are asymmetrically biased with the three resistor termination network [1]. The negative MVB signal lines “A.Data_N” and “B.Data_N” are ~750mV more positive biased than the positive MVB signal line “A.Data_P” and “B.Data_P”. This was specified in order to guarantee fail safe signal state in case the differential lines “MVB_A” and “MVB_B” are not driven by any participants [1][2].

For most RS485 drivers on the market the minimal required ESD voltage swing (> +-1.5V) for the 54 Ohm / 50 pf test load condition (homologation) is difficult to reach [1][2] if some margin is required.

**The conclusion of this measurement report can be found on the last page of this document**

# Table of Contents

# Table of Figures



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# 3 Scope

Documentation of the measurements done in order to support the decision to select an optimum RS485 half duplex driver chip. The performance of the optical components on the functional prototype have not taken in the measurement scope, since separate documents do exist.

# 4 Abbreviations and Definitions

## 4.1 Abbreviations

| | |
|---|---|
| ASIC | Application Specific Integrated Circuit. |
| BT | Bit Time in the MVB Terminology. Normally 1BT refers to 666ns pulse length |
| DSO | Digital Storage Oscilloscope. 500 MHz Bandwidth 4..2GS LeCroy LT584M |
| D.U.T | Device Under Test |
| ESD | MVB Electrical Short Distance Bus (RS485) [1] |
| EMD | MVB Electrical Middle Distance Bus (Trafo) [1] |
| GND | The digital ground. |
| HW | Hardware. |
| MX | Maxim Integrated |
| PCB | Printed Circuit Board |
| TI | Texas Instruments |

## 4.2 Symbols

A vertical bar seen on the left/right side of the document indicates a difference in the contents compared to the previous revision. Minor changes (i.e. spelling) are not marked with this bar.

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## 4.3 Definitions

### 4.3.1 Active State

- A bar "/" at the beginning or and “N” , "n” or "#" at the end of a signal and/or pin name designates a signal that is active – asserted - if the electrical level is “low”.
- If a signal is asserted, it is activated. This is independent of the level.
- If a signal is negated, it is not active. This is independent of the level.
- Positive logic: the signal is asserted when the logic level is high. The logic level is ’1’.
- Negative logic: the signal is asserted when the logic level is low. The logic level is ’0’.

### 4.3.2 Bits and Byte Order

| | |
|---|---|
| Long Word | Understood as a 32-bit wide word unless specified otherwise. |
| High Word | Understood as the 16-bit wide word from the range [31..16]. |
| Low Word | Understood as the 16-bit wide word from the range [15..0]. |
| Word | Understood as a 16-bit wide word. |
| High Byte | Bit15-8 of a word. Even Byte! |
| Low Byte | Bit7-0 of a word. Odd Byte! |
| High Nibble | Bit7-4 of a Byte. |
| Low Nibble | Bit3-0 of a Byte. |
| Bit Order | Bit31 = The most significant bit (MSB). The most left bit.<br>Bit00 = The least significant bit (LSB). The most right bit. |

The terminology *low/high byte* and *even/odd byte* is used in the sense of the INTEL little endian format! When, for some reasons the MOTOROLA Big Endian format is meant it is stated explicitly!

**Little Endian Format (INTEL)**

- Low byte D[7..0] (even byte) is stored at the address location $i$.
- High byte D[15..8] (odd byte) is stored at the address location $i+1$.

## 4.4 References

### 4.4.1 Documents

[1] IEC 61375-3-1. Edition 1.0 2012-06. TCN Part 3-1: Multifunction Vehicle Bus (MVB)
[2] IEC 61375-3-2. Edition 1.0 2012-06. TCN Part 3-2: MVB conformance testing
[3] Schematic (CAD) drawings of the custom function prototype.
[4] EMD transformer datasheet “T60403-Y4021-X123” from Vacuumschmelze Germany.
[5] PROFIBUS RS-485 TRANSCEIVERS. SN65HVD1176D. Texas Instruments.
[6] High-ESD Profibus RS-485 Transceiver. MAX14770EGSA+. Maxim Integrated.

# 5 General Test Setup

## 5.1 General HW-Test Setup

The following test setup has been used in order to measure the driver behavior for two different driver chips and for two different driver modes Trafo (EMD) and RS485 (ESD). Test Fixtures A.) and B.)

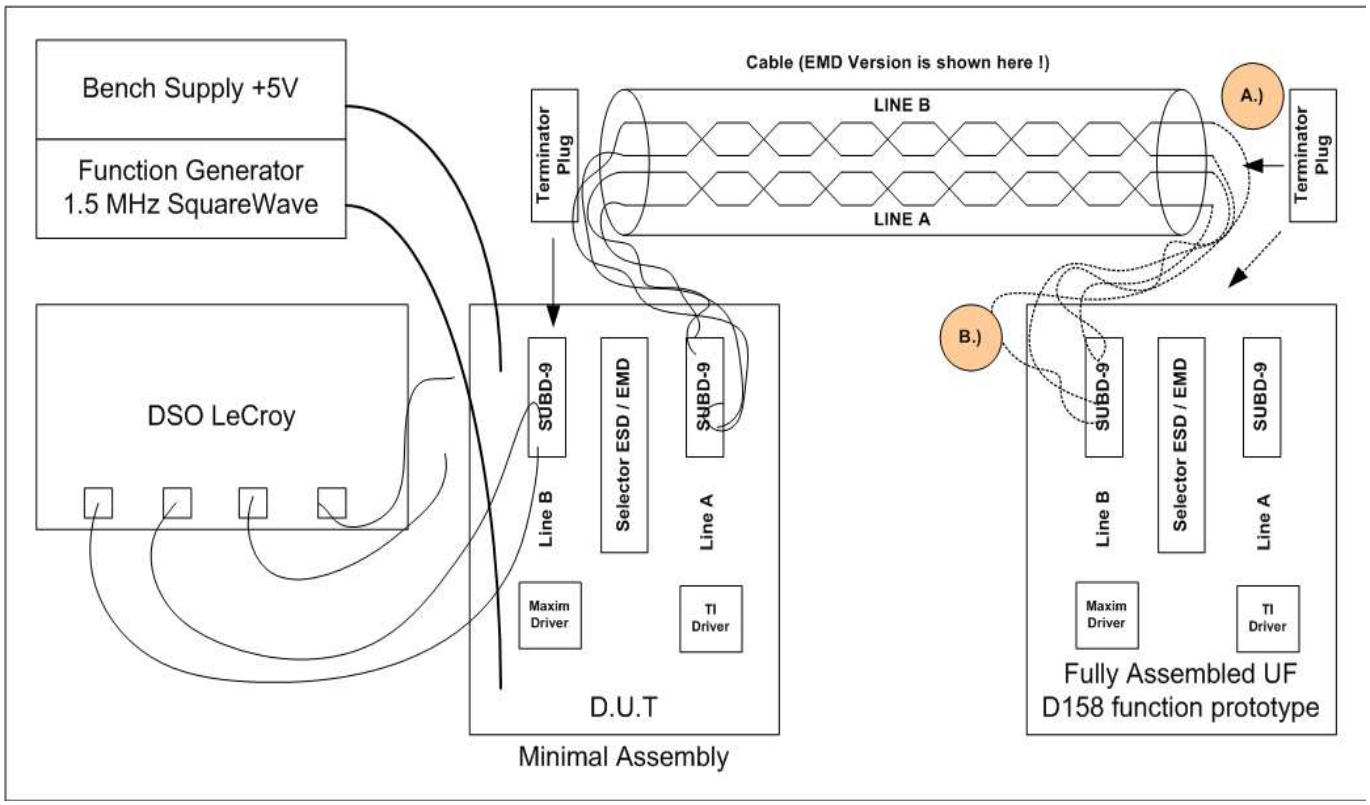


*Figure 1: HW Test Setup*

Most of the DSO 'shots' taken have been measured on the D.U.T PCB test fixture A.). In test fixture B.) a second is attached. The D.U.T is a minimally assembled function prototype that is equipped with the two RS485 driver chips and the surrounding components for ESD and EMD drive mode. The MVB line A is driven by the chip from Texas Instruments [5], the MVB line B is driven by the chip from Maxim Integrated [6].

The D.U.T has been hard-wired. It drives the lines with the signal originating from a bench signal generator in permanent mode (1.5MHz). The transmit enable control input of the driver chips on the D.U.T has been asserted permanently.

Measurements have been made on the SUBD-9 connectors of the D.U.T and after the receiver section of the second device, “the fully assembled” function prototype for test fixture B.).

Two different cables have been used, since the 'blue one' is for EMD only.

### 5.1.1 D.U.T and End Terminators for Line Termination

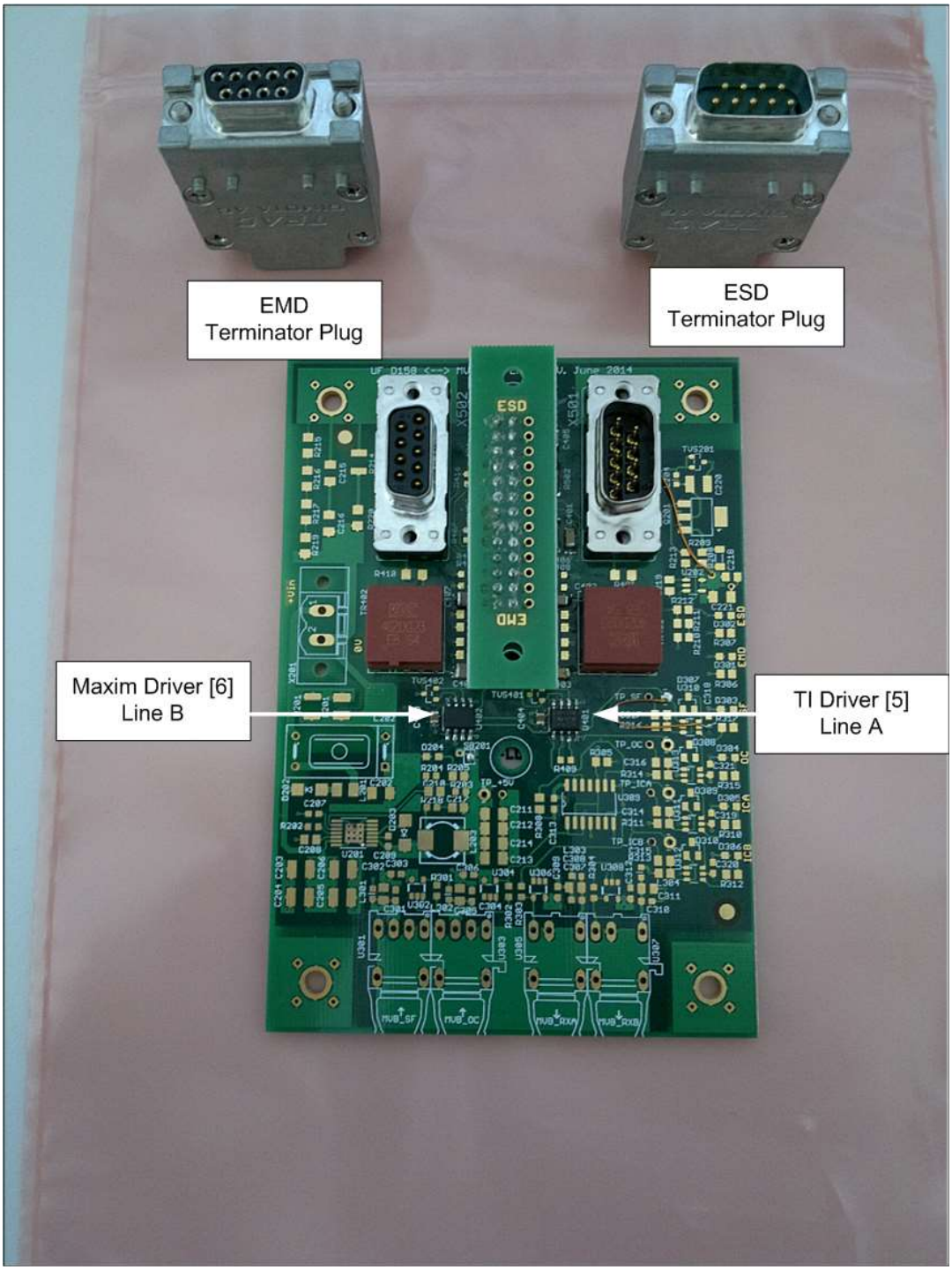


*Figure 2: D.U.T Minimal Assembly for Driver Performance Measurements*

### 5.1.2 Fully Assembled Functional Prototype


*Figure 3: Fully Assembled Functional Prototype*

### 5.1.3 Cable used for EMD Drive Measurements

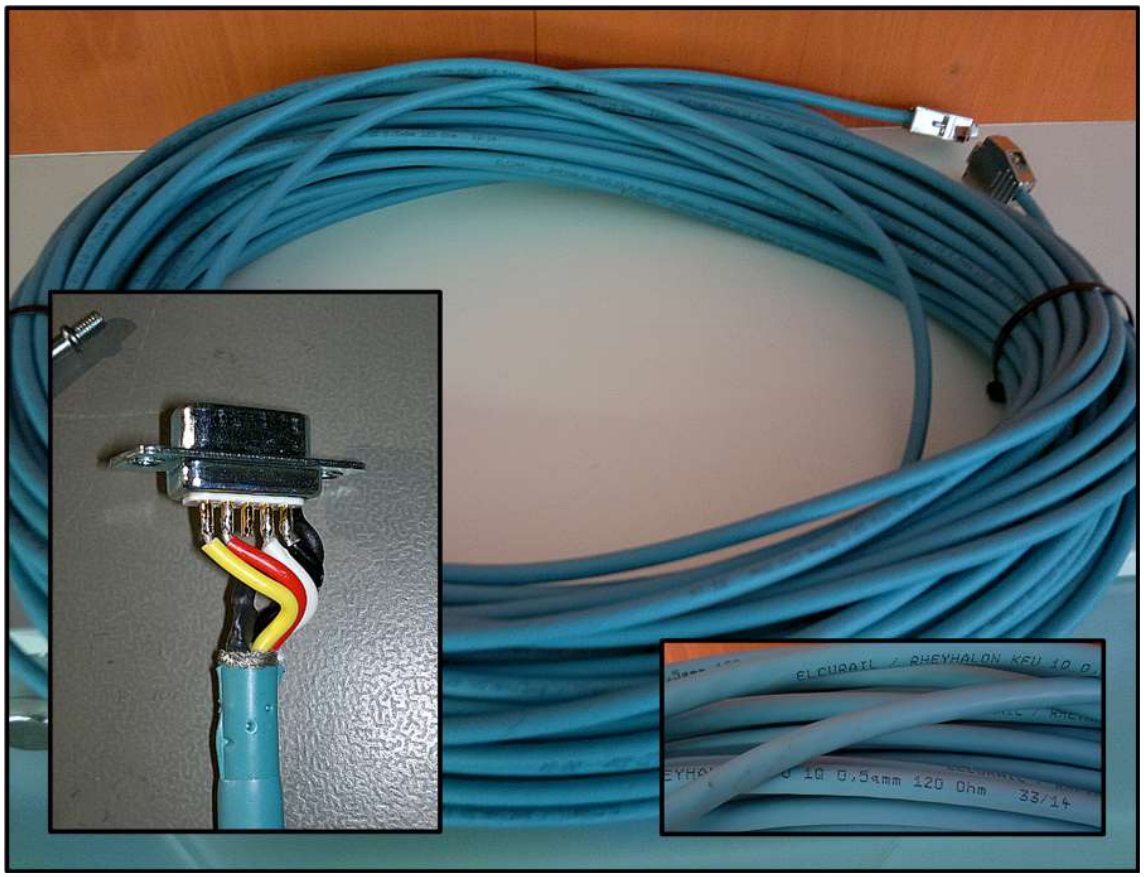

*Figure 4: MVB EMD Cable*

The blue cable has been used for EMD drive measurement only. The reason is that the internal “third wire” per differential line is missing or not soldered to the connector. ESD mode is an RS485 electrical derivative that complies with the common mode range of the RS485 specification. The common mode of the differential signaling has to be in the range of +12VDC..down to -7VDC. Without the 'third wire' which is preferable the inner shield of per differential wire-pair (one per Diff.-Line A and on per Diff.-Line B) the cable is not ESD compatible [1][2].

For this reason a cat 5 Ethernet cable (~ 50 meter cable length) has been used to measure the driver performance of the two selected driver chips in electrical ESD mode [1].

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### 5.1.4 EMD (Trafo) Drive Test including the cable


*Figure 5: EMD (Trafo) Drive Test including the cable*

### 5.1.5 ESD (RS485) Drive Test including the cable

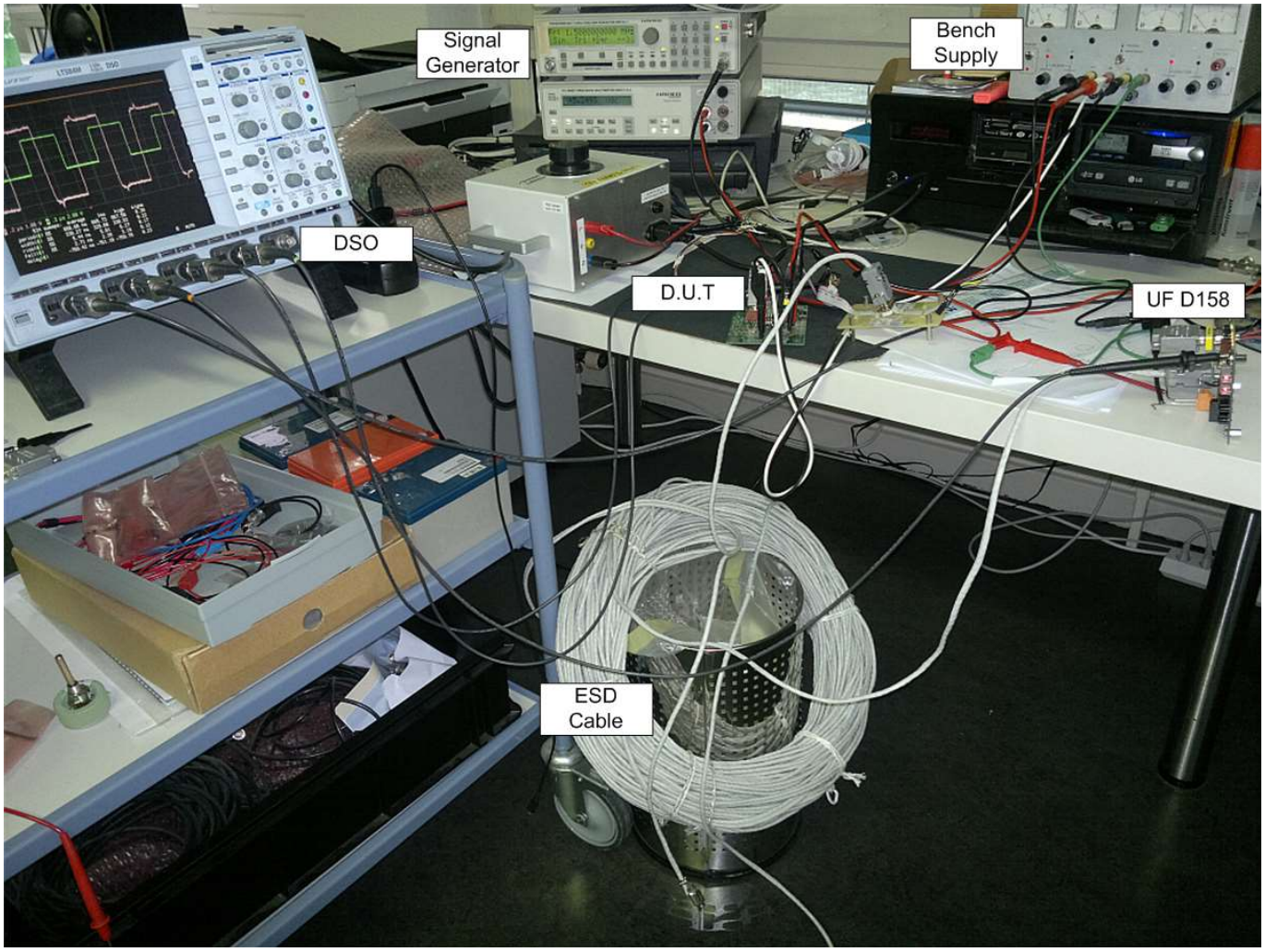


*Figure 6: ESD (RS485) Drive Test including the cable*

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# 6 Hardware Measurements

The drive and performance measurements have been made twice per driver chip. Once for the EMD mode (MVB Trafo) and once for the ESD mode (MVB RS485) [1][2]. The measurement have been started with just the D.U.T. without terminator, then including the terminator, next including the cable etc.

The last measurement (test fixture B.)) taken has been after the receiver section of the fully assembled in order to quantify the “resulting” signal and pulse width distortion. However accurate figures in the nanosecond range are difficult the measure since the signal source itself has some distortion in 2..3ns range. All the measurements have been made using single ended passive probes. The probes have been calibrated, however differential computation has been carried out on the DSO by subtracting two channels when required. Therefore signal distortion figures may have an additional tolerance. As will be seen later on the overall pulse width distortion is small compared to the 1.5MHz signal.

## 6.1 Single Ended passive Probe Setup – 10MOhm 12pF


*Figure 7: Single Ended Passive Probe Setup*

The decoder within the MVB Controller chip is able to tolerate pulse width distortion up to 3/16 BT equal ~ 120ns. The measured distortion is below 10ns and should also comply with [1] section 4.5.9.1 EMD transmitter output signal specification. Requirement f.) states a maximum deviation from the idle zero crossing line (on the cable!) to be no more than +-2% of a BT. One bit time (BT) is 666ns. Therefore +-2% is equal to ~ +-13ns.

## 6.2 MVB EMD (Trafo) Mode Transmitter Reference Waveform

The EMD transmitter reference signaling has been copied from [1] – section 4.5.9. The following properties will be discussed in the scope measurements documented here:



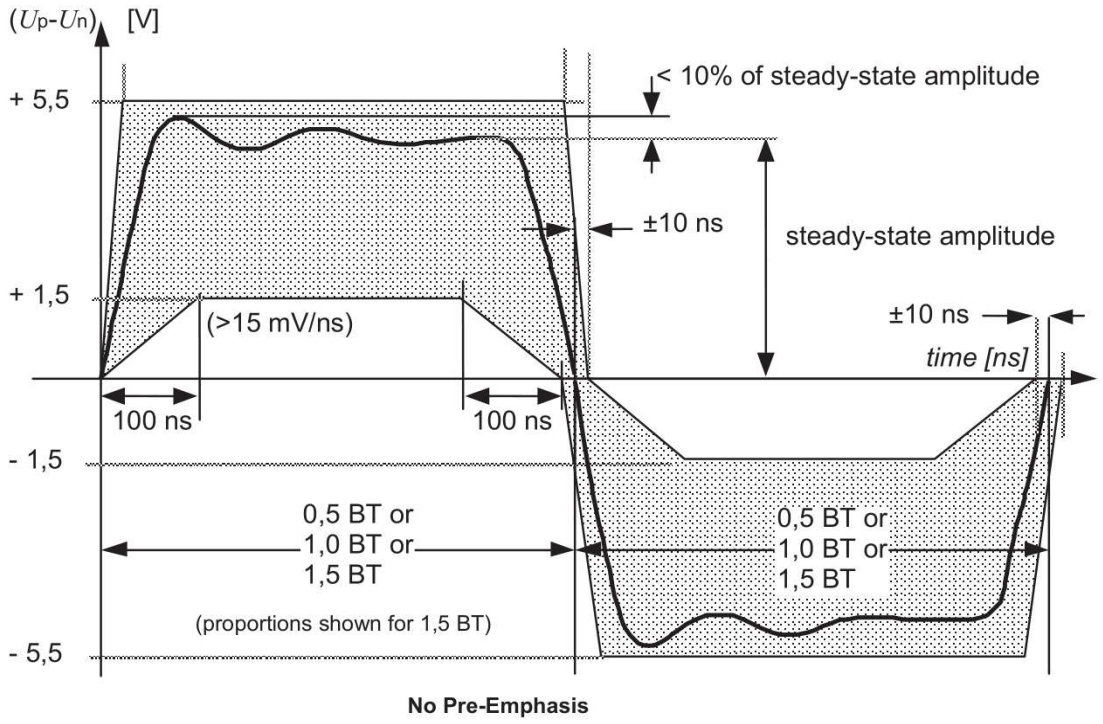


*Figure 8: MVB EMD Reference Waveform Properties -- copied from [1]*

- a.) The amplitude of the output signal shall be at least +-1.5V when connected to the heavy test circuit and at most +-5.5V when connected to the light test circuit.
- b.) The difference between the positive and the negative stationary amplitude in two consecutive pulses shall not exceed 0.10V.
- c.) The slew rate of the output signal shall be more than 15mV/ns within 0.100ns of the zero crossing.
- d.) The overshoot of the output signal, defined as the ratio of the maximum amplitude to the stationary amplitude shall not exceed 10% of its stationary amplitude.
- e.) Pulse width distortion figure (on the line!) < +-10ns. Pulse width distortion will be measured as the difference in signal rise versus signal fall time.
- f.) The edge distortion of the output signal, defined as the time difference between the idealized and the actual zero crossing, shall not exceed +-2% of one Bit Time - ~+-13ns.

## 6.3 EMD (Trafo) Mode Transmitter Measurements

### 6.3.1 D.U.T Drive Output on Line A (TI Chip) – No Termination – No Cable

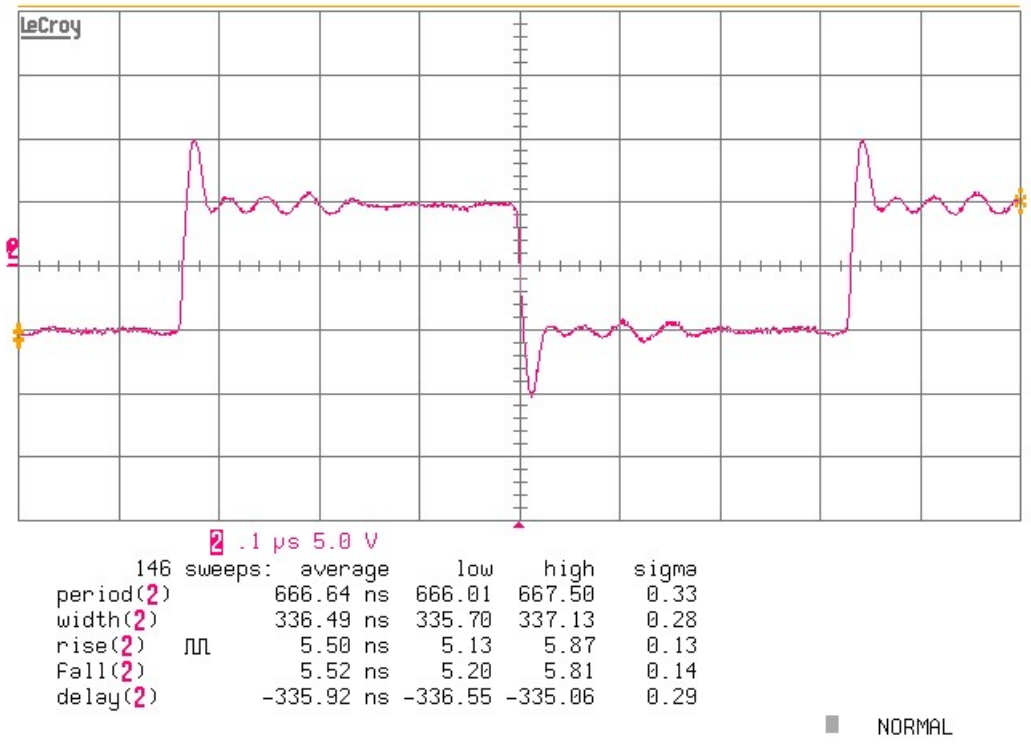


*Figure 9: EMD Line A Drive (TI Chip) - No Termination - No Cable*

The driver solution from Texas Instruments [5] (TI) features fast signal transition in the 5 ns range. This results in a significant amount of energy in the high frequency range well above the MVB 1.5MBit range resulting in ringing after the transition (Vpk ~ +-10V). Pulse width distortion after the driver measured on the SUBD-9 connector is neglect able small.

**Note:** The **unloaded transmitter** test fixture circuit is for internal use only. It will not be measured during the MVB homologation.

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### 6.3.2 D.U.T Drive Output on Line B (Maxim Chip) – No Termination – No Cable

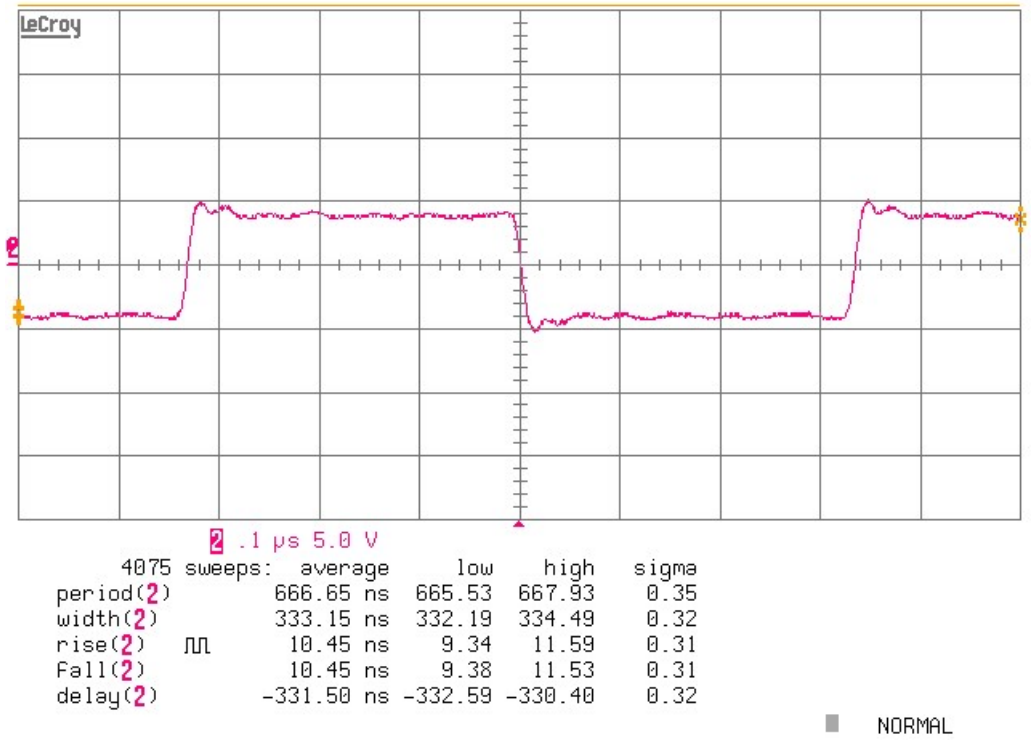


*Figure 10: EMD Line B Drive (Maxim Chip) - No Termination - No Cable*

The driver solution from Maxim Integrated [6] (MX) features fast signal transition in the 10ns range. Due to the more controlled transition no significant ringing is measured. The output signal amplitude of the unloaded differential signal is ~ +-4Vpk. The pulse width distortion after the driver measured on the SUBD-9 connector is neglect able small – 1ns range.

**Please note:** The **unloaded transmitter** test fixture circuit is for internal use only. It will not be measured during the MVB homologation.

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### 6.3.3 D.U.T Drive Output on Line A (TI Chip) – 1 Termination On – No Cable

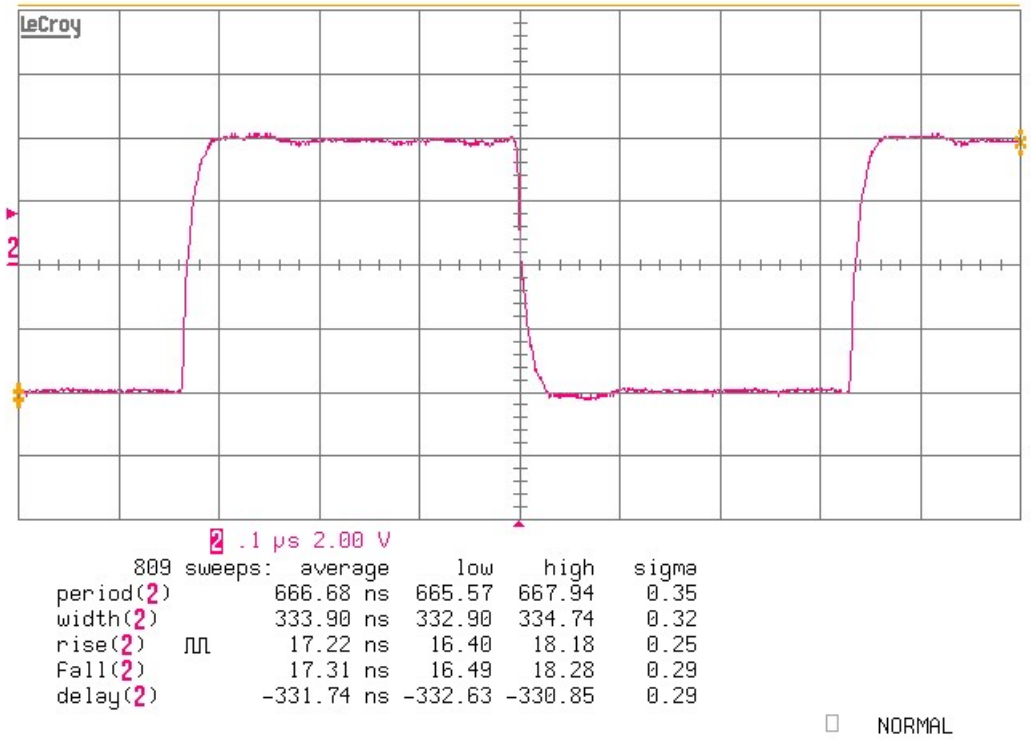


*Figure 11: EMD Line A Drive (TI Chip) – 1 Termination On ! -* ***No Cable***

The signal termination on – still no cable, shows a clean signal measured on the SUBD9 pins. Due to the terminator 120 Ohm load the amplitude is reduced to +-4Vpk. Due to the loaded output drive circuitry within the TI chip the raise and fall time has been increased to ~ 17ns.

| Req. | MVB EMD Transmitter Requirements – section 6.2 on page 13 | Result |
|---|---|---|
| | | |
| a.) | +-4Vpk | Passed |
| b.) | Symmetrical (difficult to measure 100mVdifference in amplitude | (Passed) |
| c.) | The slew rate is in the range of ~ 400mV / ns | Passed |
| d.) | The overshoot is < 400mV or 10% of the steady state signal amplitude | Passed |
| e.) | The pulse width distortion $t_{rise} – t_{fall}$ is ~ 2ns and smaller than +-10ns | Passed |
| f.) | The edge distortion is below ~ +-13ns (< 2% of 1BT) | Passed |

### 6.3.4 D.U.T Drive Output on Line B (MX Chip) – 1 Termination On – No Cable

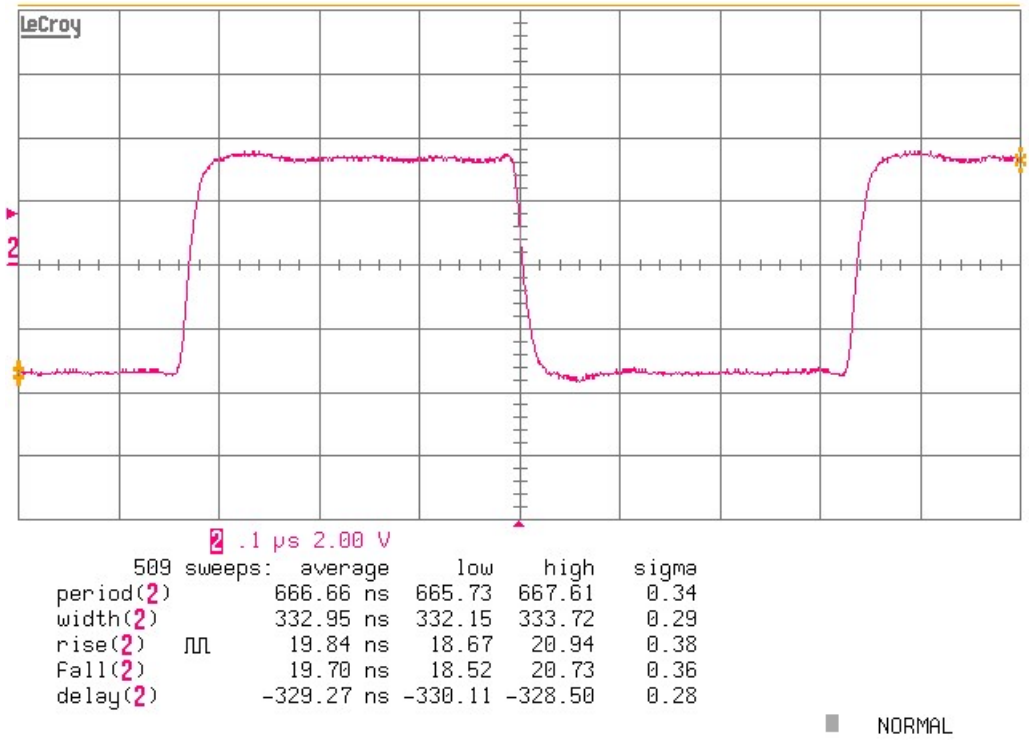


*Figure 12: EMD Line B Drive (MX Chip) – 1 Termination On ! -* ***No Cable***

The signal termination on – still no cable, shows a clean signal measured on the SUBD9 pins. Due to the terminator 120 Ohm load the amplitude is reduced to ~ +-3.6Vpk. Due to the loaded output drive circuitry within the TI chip the raise and fall time has been increased to ~ 20ns.

| Req. | MVB EMD Transmitter Requirements – section 6.2 on page 13 | Result |
|---|---|---|
| | | |
| a.) | ~ +-3.6Vpk | Passed |
| b.) | Symmetrical (difficult to measure 100mVdifference in amplitude | (Passed) |
| c.) | The slew rate is in the range of ~ 360mV / ns | Passed |
| d.) | The overshoot is < 360mV or 10% of the steady state signal amplitude | Passed |
| e.) | The pulse width distortion $t_{rise} – t_{fall}$ is ~ 2ns and smaller than +-10ns | Passed |
| f.) | The edge distortion is below ~ +-13ns (< 2% of 1BT) | Passed |

### 6.3.5 D.U.T Drive Output on Line A (TI Chip) – with Cable terminated

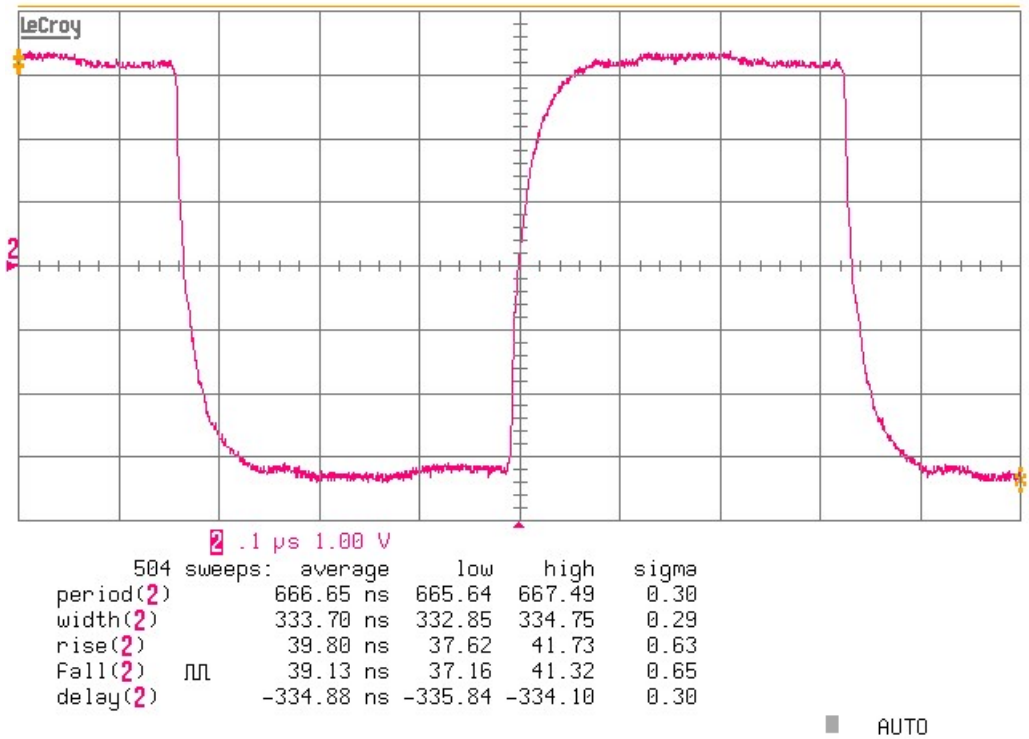


*Figure 13: D.U.T Drive Output on Line A (TI Chip) – with Cable terminated*

**Note:** The vertical resolution has been increased to 1 volt per division. The cable in test fixture A.) is terminated on both ends using 2×120 Ohm per differential signal pair.

| Req. | MVB EMD Transmitter Requirements – section 6.2 on page 13 | Result |
|---|---|---|
| | | |
| a.) | ~ +-3.2Vpk | Passed |
| b.) | Symmetrical < 100mV in amplitude | (Passed) |
| c.) | The slew rate is in the range of ~ 160mV / ns | Passed |
| d.) | The overshoot is < 320mV or 10% of the steady state signal amplitude | Passed |
| e.) | The pulse width distortion $t_{rise} – t_{fall}$ is ~ 4ns and smaller than ~ +-10ns | Passed |
| f.) | The edge distortion is below ~ +-13ns (< 2% of 1BT) | Passed |

### 6.3.6 D.U.T Drive Output on Line B (MX Chip) – with Cable terminated

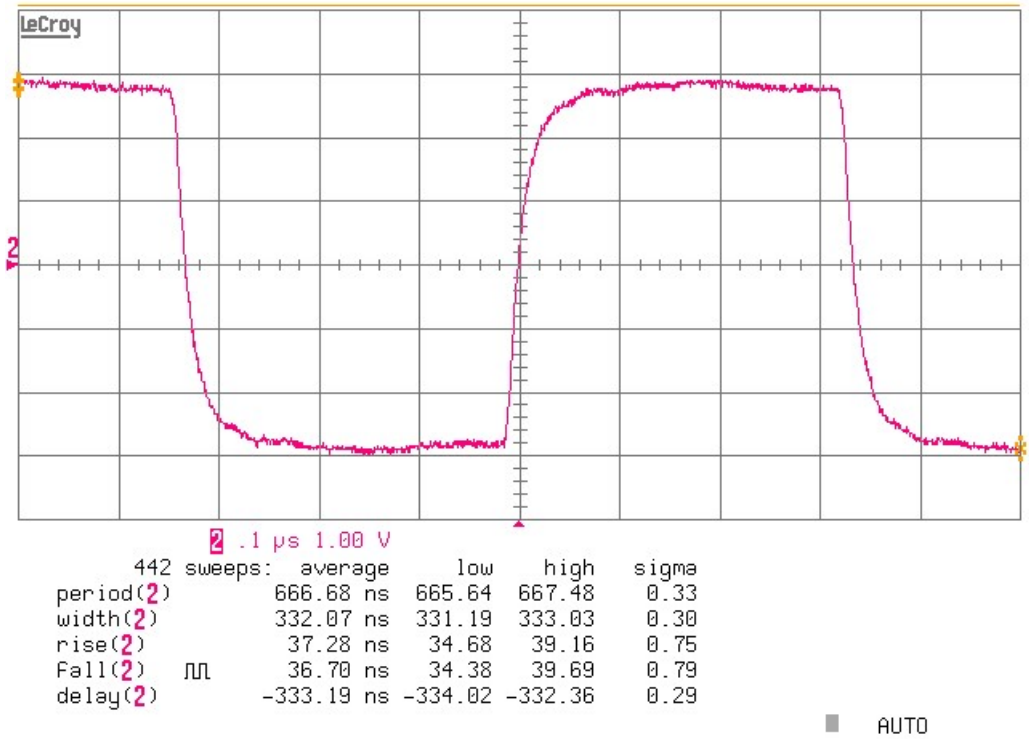


*Figure 14: D.U.T Drive Output on Line B (MX Chip) – with Cable terminated*

**Note:** The vertical resolution has been increased to 1 volt per division. The cable in test fixture A.) is terminated on both ends using 2×120 Ohm per differential signal pair.

| Req. | MVB EMD Transmitter Requirements – section 6.2 on page 13 | Result |
|---|---|---|
| | | |
| a.) | ~ +-2.8Vpk | Passed |
| b.) | Symmetrical < 100mV in amplitude | (Passed) |
| c.) | The slew rate is in the range of ~ 160mV / ns | Passed |
| d.) | The overshoot is < 280mV or 10% of the steady state signal amplitude | Passed |
| e.) | The pulse width distortion $t_{rise}$ – $t_{fall}$ is ~ 5ns and smaller than ~ +-10ns | Passed |
| f.) | The edge distortion is below ~ +-13ns (< 2% of 1BT) | Passed |

### 6.3.7 RS485 Receiver Output 2nd UF D150 Line A (TI Chip) – with Cable terminated

The signal has been captured after the RS485 Transceiver on the second fully assembled function prototype.

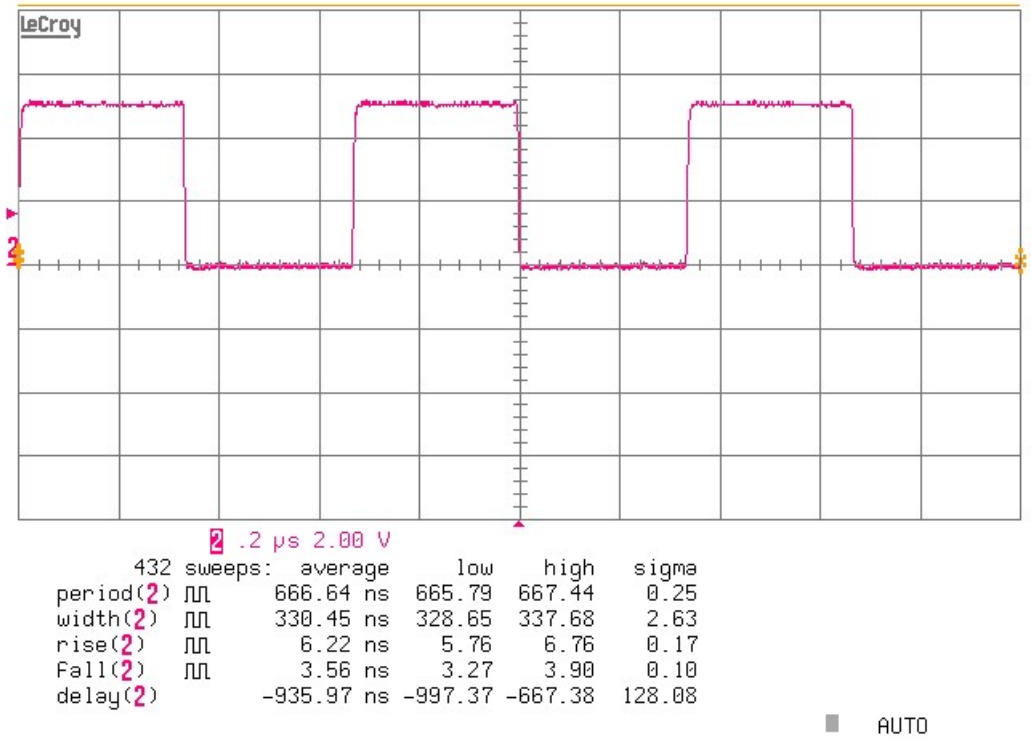


*Figure 15: RS485 RX Output 2nd UF D150 Line A (TI Chip) – with Cable*

Some signal pulse width distortion seems to visible. It is in the one digit ns range. The signal source itself has some errors. The measured and “decoded” pulse width distortion is ~ +-5ns. This is small compared to the tolerable distortion the MVB decoder IP is capable to handle – max. 3BT ~ 100ns.

However the test fixture B.) has only two physical layer participants compared to a real MVB network with many different nodes from many different vendors. For this reason it is mandatory to the keep the overall distortion as small as possible.

**Note:** The test fixture B.) is for internal use only. It will not be measured during the MVB homologation.

### 6.3.8 RS485 Receiver Output 2nd UF D150 Line B (MX Chip) – with Cable terminated

The signal has been captured after the RS485 Transceiver on the second fully assembled function prototype.

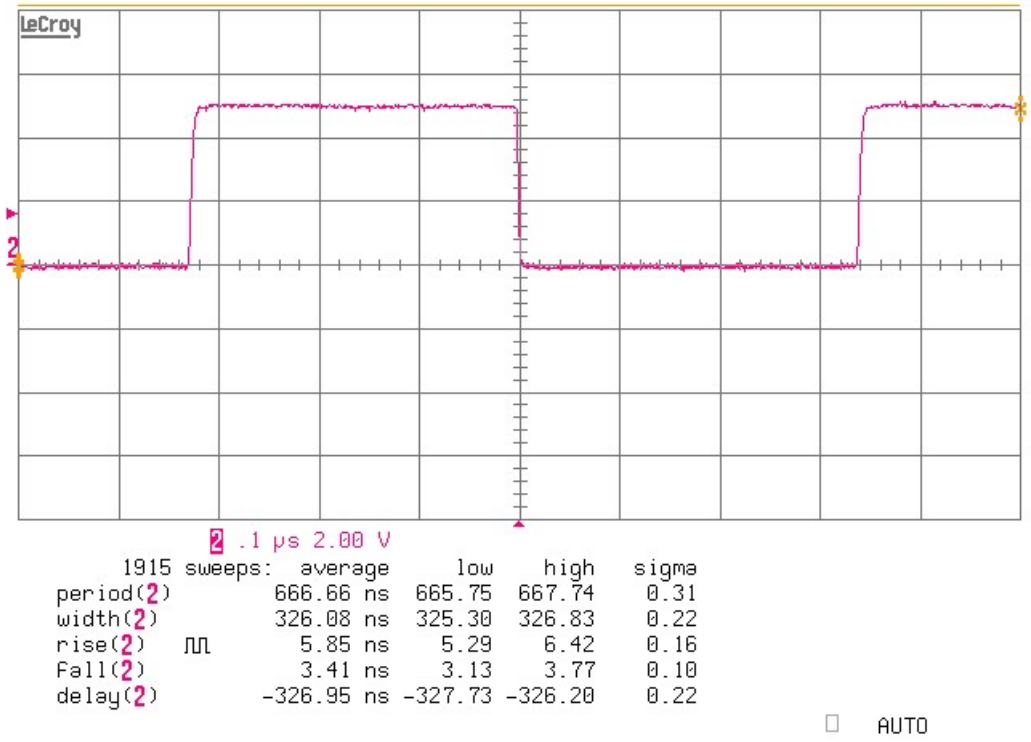


*Figure 16: RS485 RX Output 2nd UF D150 Line B (MX Chip) – with Cable*

Some signal pulse width distortion seems to visible. It is in the one digit ns range. The signal source itself has some errors. The measured and “decoded” pulse width distortion is ~ +-7ns. This is small compared to the tolerable distortion the MVB decoder IP is capable to handle – max. 3BT ~ 100ns.

However the test fixture B.) has only two physical layer participants compared to a real MVB network with many different nodes from many different vendors. For this reason it is mandatory to the keep the overall distortion as small as possible.

**Note:** The test fixture B.) is for internal use only. It will not be measured during the MVB homologation.

### 6.3.9 EMD Signal Integrity Issue Measuring End to End

From the previous measurements the probability is high that both devices [5][6] may be used for EMD mode. Driver performance is not 100% the same however the deviations are small but good enough to pass MVB class 1 homologation.

**Signal Integrity**

Measuring End-to-End in test fixture B.) however shows some weakness of the actual implementation that requires improvement in the second prototype run! This signal integrity issue originates do to badly matched impedance of the differential signal pairs between the configuration connector and the stub traces of the PCB towards the EMD signal source!

**Note:** This imperfection may not be visible during homologation, since **all** measurements are taken at the D.U.T side. During homologation the “remote” MVB node is the 'golden' perfect device from Bombardier/Siemens with no impedance mismatch to “travel back” the line towards the source!

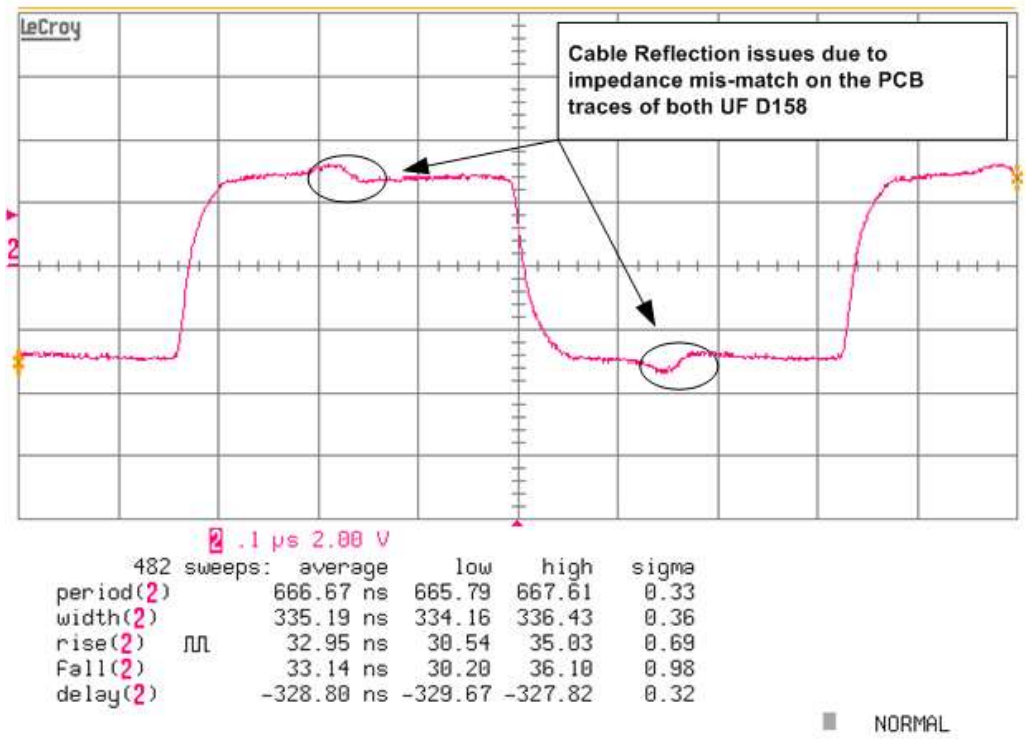


*Figure 17: EMD Mode Minimal Signal Integrity Issue*

This minimal reflections shall be removed by properly designing the “diff. strip lines without ground plane” (120 Ohm diff. Impedance) on the PCB!

## 6.4 MVB ESD (RS485) Mode Transmitter Reference Waveform

As a general remark, the interface is based on the RS 485 (ISO 8482) specification, with the addition of biasing. The ESD transmitter reference signaling has been copied from [1] – section 4.4.7 and 4.4.8. The following properties will be discussed in the scope measurements documented here:

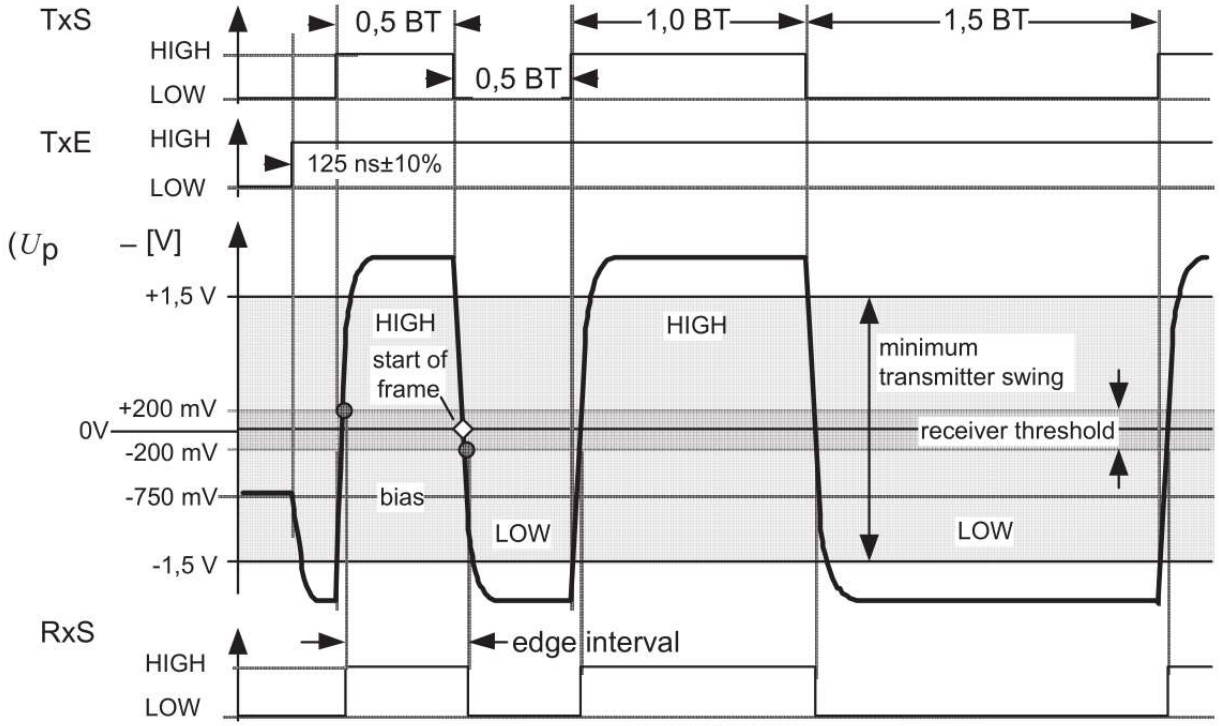


**Figure 10 – Example of start of frame (ESD)**

*Figure 18: MVB ESD Reference Waveform Properties -- copied from [1]*

a.) The rise time of the signal (10 % – 90 %) shall be less than 0,03 BT (< 20,0 ns at 1,5 Mb/s), when driving a load of 54,0 Ohm in parallel with 50,0 pF.

b.) The transmitter shall provide a low impedance differential voltage source with two active levels

***HIGH Level:*** when the voltage difference (U p – U n) is within +1.5 V < (U p – U n) < +5.0 V when driving a resistive load of 54,0 Ohm, and +1.5 V < (U p – U n) < +6.0 V when unloaded.

***Low Level:*** when the voltage difference (U p – U n) is within -1.5 V > (U p – U n) > -5.0 V when driving a resistive load of 54,0 Ohm, and -1.5 V > (U p – U n) > -6.0 V when unloaded.

NOTE Since this specification is stricter than ISO/IEC 8482, care should be taken in selecting commercial transceivers. This specification is fulfilled by transmitters which conform to IEC 61158-2

### 6.4.1 D.U.T Drive Output on Line A (TI Chip) – Unloaded

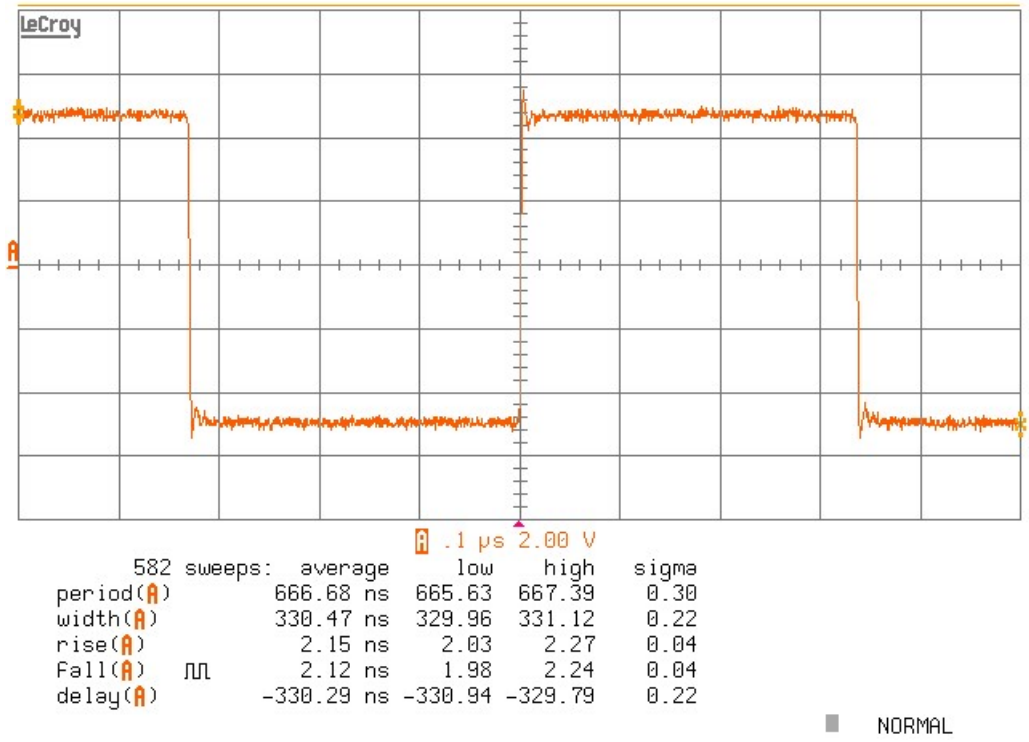


*Figure 19: ESD D.U.T Drive Output on Line A (TI Chip) – Unloaded*

The transmitter from TI [5] in ESD mode features a nearly ideal signal waveform. The duty cycle deviation from ideal originates mostly from the imperfect signal source. The signal rise and fall time figures are almost the same. The transmitter output swing approaches rail to rail in the unloaded condition ~ +-5Vpk.

**Note:** The **unloaded transmitter** test fixture circuit is for internal use only. It will not be measured during the MVB homologation. During homologation the D.U.T is a MVB slave device. It will respond only if the MVB master is source addressing the MVB slave.

### 6.4.2 D.U.T Drive Output on Line B (MX Chip) – Unloaded

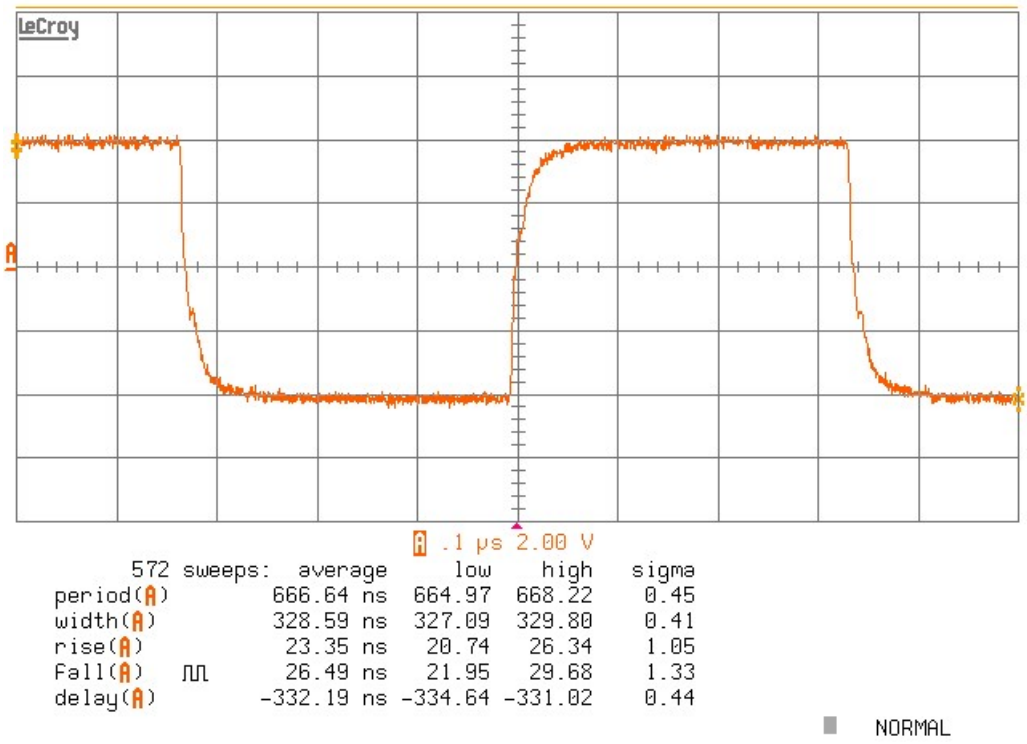


*Figure 20: ESD D.U.T Drive Output on Line B (MX Chip) – Unloaded*

The transmitter from Maxim [6] in ESD features a nice signal waveform too. However the internal driver architecture is different from the TI solution, since the rise and fall times are pretty slow in the absence of an external termination network. The transmitter output swing approaches rail to rail in the unloaded condition ~ +-4Vpk.

**Note:** The **unloaded transmitter** test fixture circuit is for internal use only. It will not be measured during the MVB homologation. During homologation the D.U.T is a MVB slave device. It will respond only if the MVB master is source addressing the MVB slave.

### 6.4.3 D.U.T Drive Output on Line A (TI Chip) – Biased and Loaded with 120 Ohm

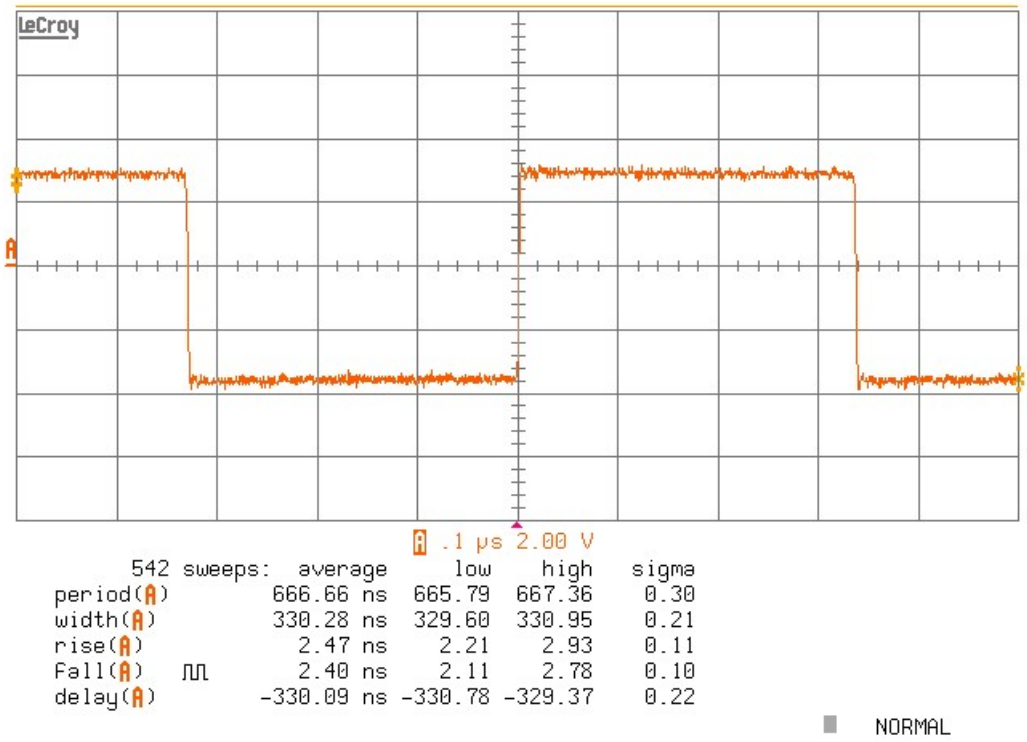


*Figure 21: ESD D.U.T. Lina A (TI Chip) - Biased with 120 Ohm Load*

| Req. | MVB ESD Transmitter Requirements – section 6.4on page 23 | Result |
|---|---|---|
| | | |
| a.) | The rise and fall time is 2.5ns and below 20ns. However the nominal load is not high enough. | n.a. |
| b.) | Voltage swing is within allowed boundaries ~+2.8V...-3.6V | (Passed) |

### 6.4.4 D.U.T Drive Output on Line B (MX Chip) – Biased and Loaded with 120 Ohm

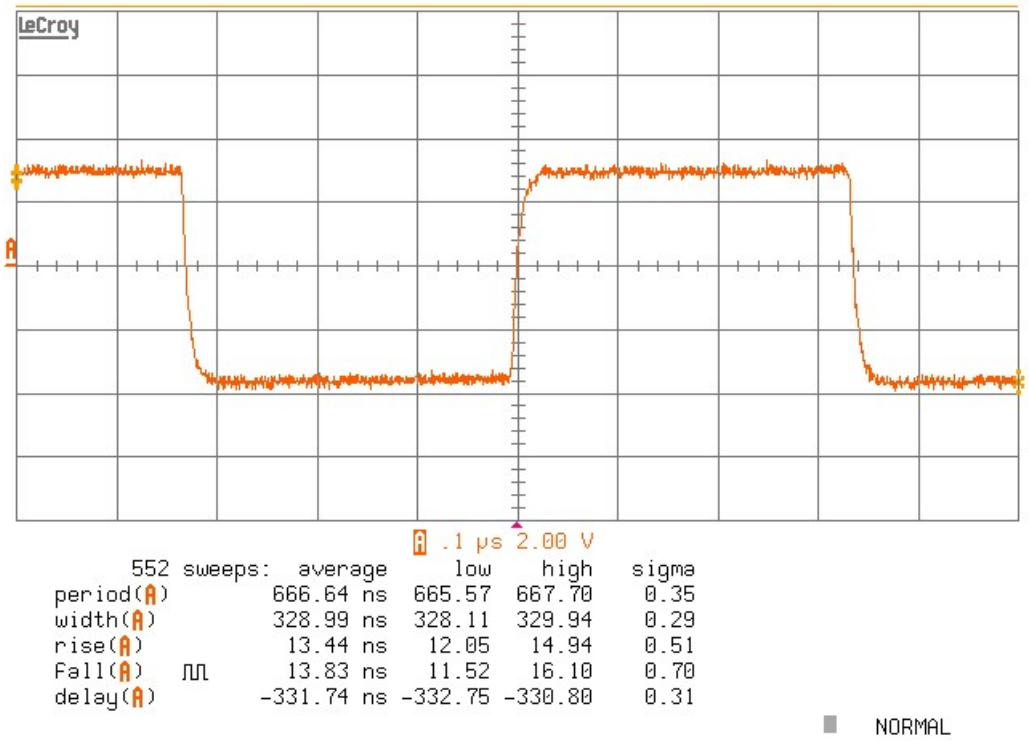


*Figure 22: ESD D.U.T. Lina B (MX Chip) - Biased with 120 Ohm Load*

| Req. | MVB ESD Transmitter Requirements – section 6.4on page 23 | Result |
|---|---|---|
| | | |
| a.) | The rise and fall time is 13..16 ns and below 20 ns. However the nominal load is not high enough. | n.a. |
| b.) | Voltage swing is within allowed boundaries ~+2.8V...-3.6V | (Passed) |

### 6.4.5 D.U.T Drive Output on Line A (TI Chip) – Biased and Loaded with 60 Ohm

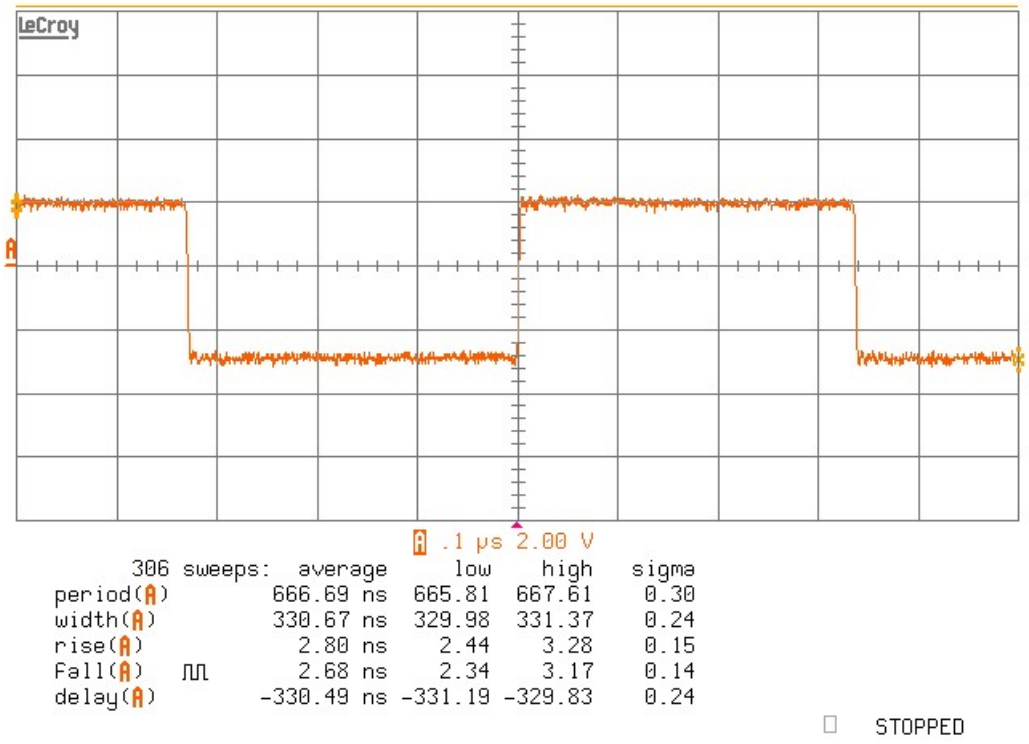


*Figure 23: ESD D.U.T. Lina A (TI Chip) - Biased with 60 Ohm Load*

| Req. | MVB ESD Transmitter Requirements – section 6.4on page 23 | Result |
|---|---|---|
| | | |
| a.) | The rise and fall time is ~ 3ns and below 20 ns. The is close to the requested test load of 54 Ohm. | (Passed) |
| b.) | Voltage swing is within allowed boundaries ~+2.0V...-2.8V | (Passed) |

### 6.4.6 D.U.T Drive Output on Line B (MX Chip) – Biased and Loaded with 60 Ohm

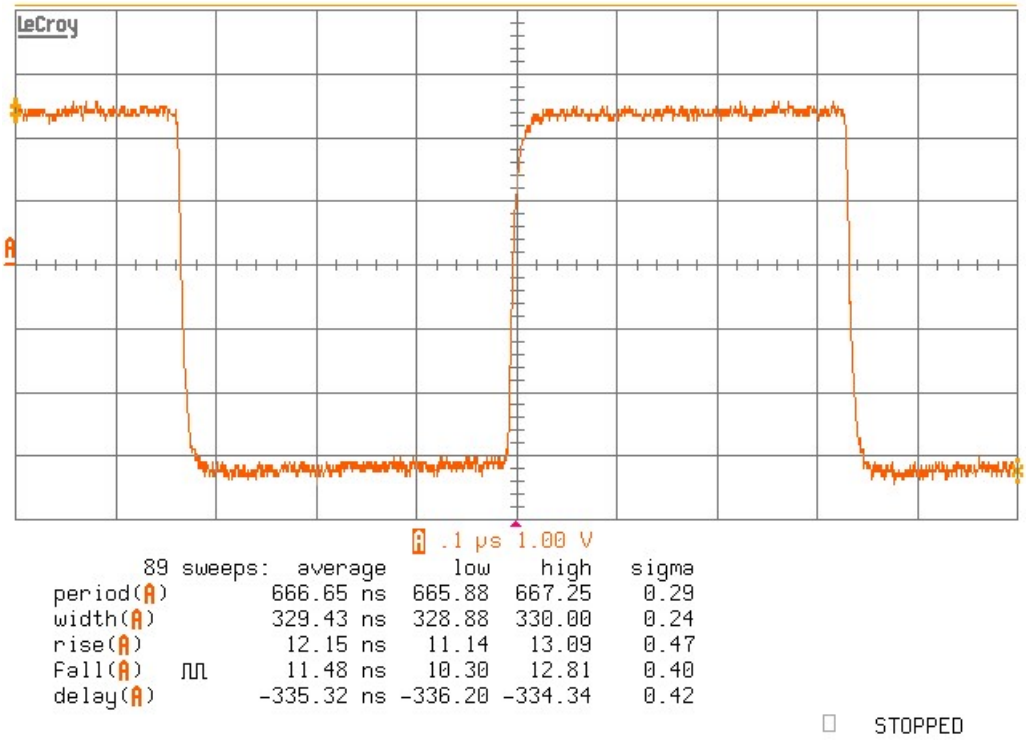


*Figure 24: ESD D.U.T. Lina B (MX Chip) - Biased with 60 Ohm Load*

Please Note: The vertical resolution has been set to 1V/Division

| Req. | MVB ESD Transmitter Requirements – section 6.4on page 23 | Result |
|---|---|---|
| | | |
| a.) | The rise and fall time is ~ 11ns and below 20 ns. The is close to the requested test load of 54 Ohm. | (Passed) |
| b.) | Voltage swing is within allowed boundaries ~+2.4V...-3.2V | (Passed) |

It is interesting to note that the transmitting driving power is better than for the TI solution.

### 6.4.7 D.U.T Drive Output on Line A (TI Chip) – with Cable terminated

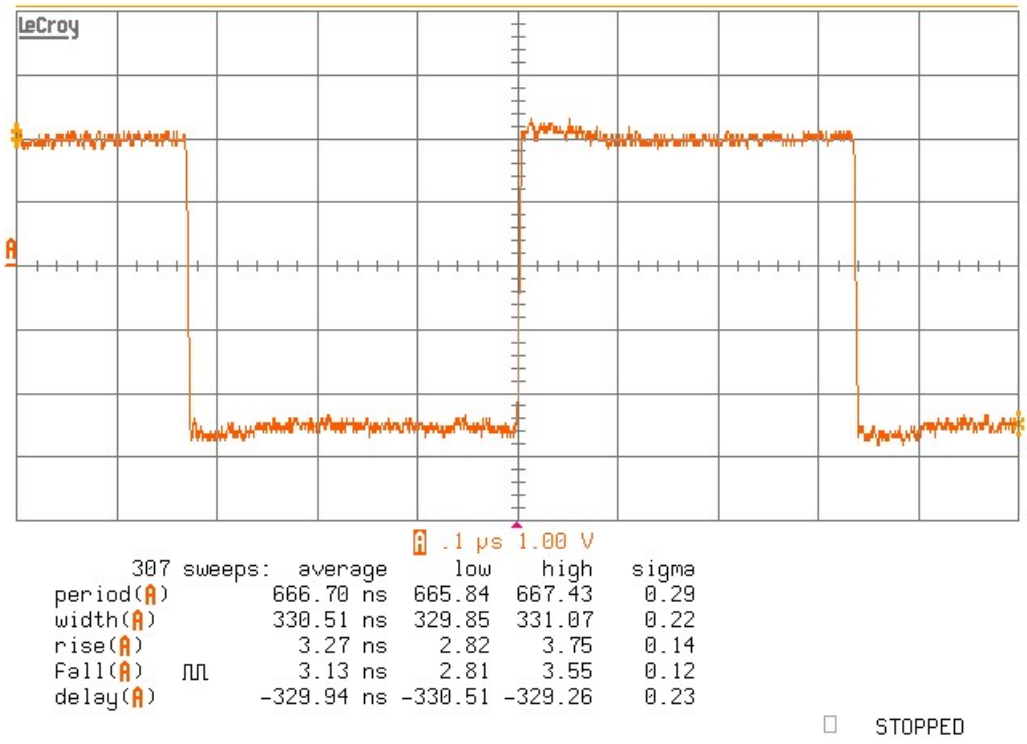


*Figure 25: ESD D.U.T. Lina A (TI Chip) - with Cable terminated*

Please Note: The vertical resolution has been set to 1V/Division

| Req. | MVB ESD Transmitter Requirements – section 6.4on page 23 | Result |
|---|---|---|
| | | |
| a.) | The rise and fall time is ~ 3..4ns and below 20 ns. The is close to the requested test load of 54 Ohm. | (Passed) |
| b.) | Voltage swing is within allowed boundaries ~+2.0V...-2.7V | (Passed) |

### 6.4.8 D.U.T Drive Output on Line B (MX Chip) – with Cable terminated

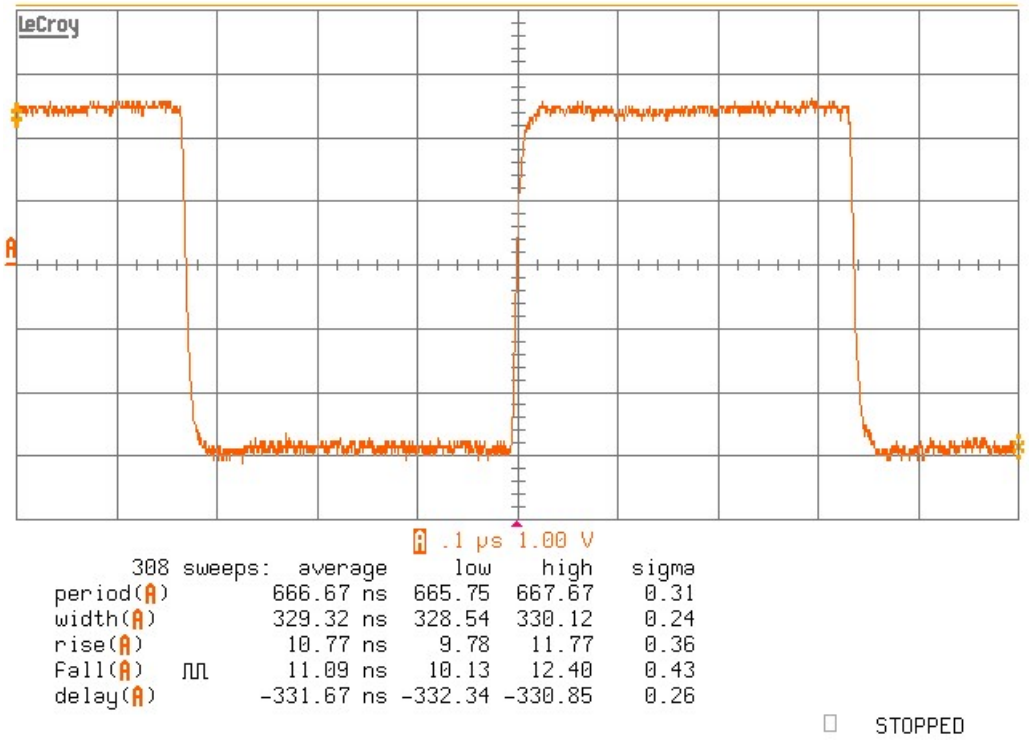


*Figure 26: ESD D.U.T. Lina B (MX Chip) - with Cable terminated*

Please Note: The vertical resolution has been set to 1V/Division

| Req. | MVB ESD Transmitter Requirements – section 6.4on page 23 | Result |
|---|---|---|
| | | |
| a.) | The rise and fall time is ~ 11ns and below 20 ns. The is close to the requested test load of 54 Ohm. | ( Passed ) |
| b.) | Voltage swing is within allowed boundaries ~+2.4V...-3.0V | ( Passed ) |

Superior performance in terms of voltage swing while rise and fall times are about 50% of the tolerated 20ns. For ESD the Chip from Maxim Integrated is the preferred solution.

### 6.4.9 ESD Signal Integrity Issue Measuring End to End

Using test fixture B.) some peaking due to badly matched differential traces on the function prototype is visible. The conslusion is the same as stated earlier. Read 6.3.9 on page 22. A two dimenstional field solver may be used to better match the differential trace impedance being ~ 120 Ohm. Then the peaking due to reflection will disapear.

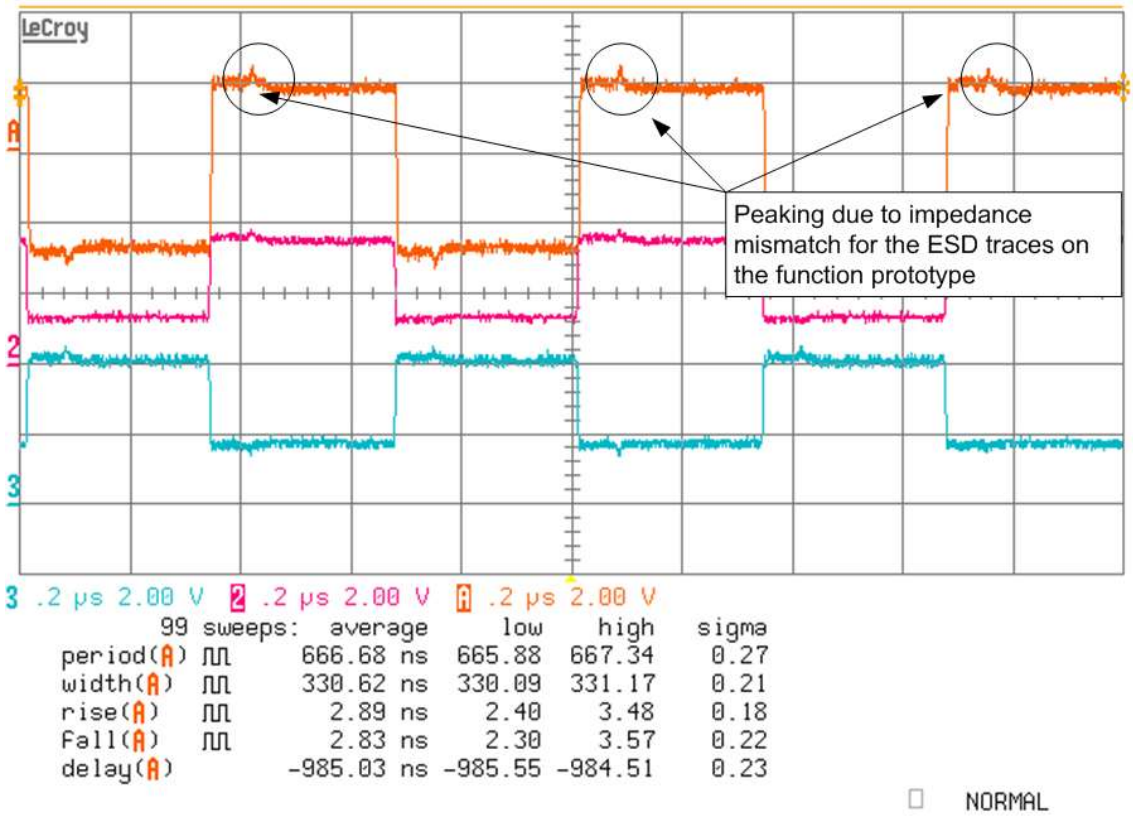


*Figure 27: ESD Mode Minimal Signal Integrity Issue (TI Chip)*

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# 7 Conclusion

## Chip Selection

The selected RS485 half-duplex transceivers from Texas Instruments [5] and from Maxim Integrated [6] are both possible solutions to fulfill the MVB requirements regarding EMD and ESD transmitter driver requirements. However if one has to be selected the device from Maxim Integrated is the better choice. It features slower rise and fall times, still within the specified tolerance band, and provides stronger drive and higher voltage swing for the more difficult ESD mode under heavy load.

Still the solution from TI may be used as second source even if the ESD voltage swing is 0.4..0.5V lower but still about ~300..400mV higher than the specified minimum [1][2]. The rise and fall times from the TI solutions are very fast. Any signal integrity issues will therefore show up notable.

## Signal Integrity

For the second prototype run the differential traces on the PCB must be routed more carefully. Due to space constraints vertical stacking as opposed to edge coupled strip lines may be used. This is more difficult to handle and requires careful specification of the PCB layer stacking details as well as the use of a two dimensional field solver. The differential impedance shall be matched to be 120 Ohm. The small exception where this might not be possible is the configuration connector. However this is a very short trace length and can be omitted regarding the computation of the required trace width and distance to each other.

# 8 Revision History

| Revision | Date | Name | Remarks |
|---|---|---|---|
| Initial Version | 26-09-2014 | M.Meng | -- |
| | | | |

Meng Engineering
Ennetbaden 26.09.2014